PCIE Bus Quad Serial Ports and Print Port Chip CH384

Datasheet (I)

Version: 1A

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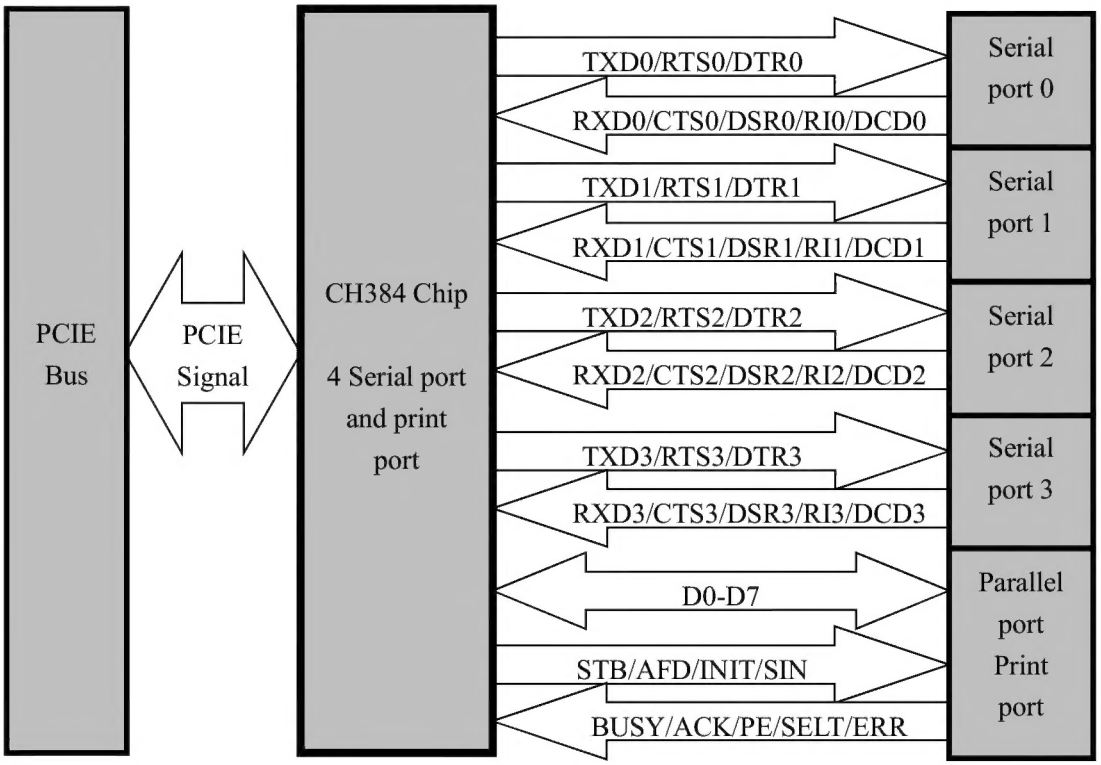
1. Overview

CH384 is a PCI-Express bus based on Quad serial ports and print port chip. It includes 4 UARTs compatible with 16C550 or 16C750 and an EPP/ECP enhanced bidirectional parallel port. It can also be expanded with an additional CH438 chip to up to 24 serial ports. UART provides an independent 256-byte FIFO buffer for transmitting and receiving, supports IrDA infrared codec, supports communication baud rate up to 8Mbps, and can be used for RS232 serial port expansion of the PCIE bus, PCIE high-speed serial port with automatic hardware rate control, and serial port group network, RS485 communication, IrDA communication, parallel port/print port expansion, etc. The figure below is its general application block diagram.



2. Feature

2.1 Overview

- The same chip can be configured as a 4-channel serial port plus a parallel/print port or a 4-channel serial port plus an extended multi-serial port on the PCIE bus.
- Provide a 2-wire serial host interface, which can be connected to a serial EEPROM device similar to 24C0X for storing non-volatile data.
- The device identification of the PCIE board can be set in the EEPROM device (Vendor ID, Device ID, Class Code, etc.)
- The driver supports Windows 98/ME/NT4.0/2000/XP/Vista/Win7/Server2003 and Linux.
- 3.3V power supply voltage, I/O pins support 5V tolerant voltage, and support serial port low-power sleep mode.

- The chip function is equivalent to CH367 chip plus CH438 chip, providing 8 serial ports, 16 serial ports, 28 serial ports and other application solutions.
- LQFP-100 lead-free package, RoHS compliant.

2.2 Serial Port

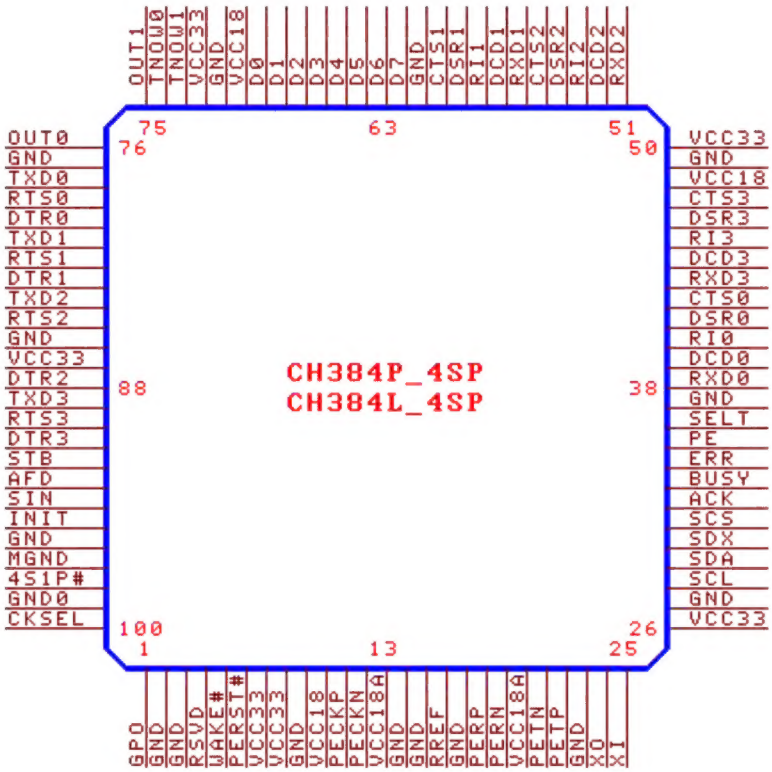
- Fully independent 4 asynchronous serial ports, compatible with 16C550, 16C552, 16C554 and 16C750 with enhancements.
- Support 5, 6, 7 or 8 data bits and 1 or 2 stop bits.
- Support odd, even, no check, blank 0, flag 1 and other check modes.
- Programmable communication baud rate, support 115200bps and up to 8Mbps.
- Built-in 256-byte FIFO buffer, support 4 FIFO trigger stages.
- Support MODEM signals CTS, DSR, RI, DCD, DTR, RTS, which can be converted to RS232 level.
- Support automatic handshake and automatic transmission rate control of hardware flow control signals CTS and RTS, compatible with TL16C550C.
- Support serial port frame error detection and Break line interval detection.
- Support full-duplex and half-duplex serial communication.
- Serial port 0 has built-in SIR infrared codec, supports IrDA infrared communication with baud rate from 2400bps to 115200bps.
- Support external CH438 chip to expand another 8 to 24 asynchronous serial ports, realizing PCIE eight serial ports and PCIE twenty-eight serial ports.

2.3 Parallel Port

- Support SPP, Nibble, Byte, PS/2, EPP, ECP, and other IEEE1284 parallel/print port operating modes.
- Support bi-directional data transmission and up to 1M bytes per second.

3. Package

4 Serial ports + Parallel port



For application instructions and pin diagrams of 4 serial ports + extended multi-serial ports, please refer to datasheet (II) CH384DS2.PDF.

Package Form	Shaping Width	Pin Spacing		Package Description	Order Model
LQFP100	14mm × 14mm	0.5mm	19.7mil	Low Profile Quad Flat Pack	CH384P
LQFP100	14mm × 14mm	0.5mm	19.7mil	Low Profile Quad Flat Pack	CH384L

Note: CH384P has a single externally supplied 3.3V supply and a built-in 3.3V to 1.8V LDO step-down regulator, eliminating the need for an externally supplied 1.8V;

CH384L requires external 3.3V supply and 1.8V supply.

4. Pin

4.1 Power Line

Pin No.	Pin Name	Type	Pin Description
7,8,26,50,72,87	VCC33	Power	3.3V I/O power
10,48,70	VCC18	Power	1.8V core power
13,20	VCC18A	Power	1.8V transmitting power
97,2,3,9,14,15,17,23,27, 37,49,61,71,77,86,96,99	GND	Power	Common ground

4.2 PCIE Bus Signal Line

Pin No.	Pin Name	Type	Pin Description
6	PERST#	Input	System reset signal line, active low
11,12	PECKP/PECKN	Input	System reference clock differential input
18,19	PERP/PERN	PCIE input	PCIE receiver differential signal input
22,21	PETP/PETN	PCIE output	PCIE transmitter differential signal output
5	WAKE#	Open-drain output	Bus wake-up output, active at low level, not connected if not used

4.3 Serial Port 0 ~ 3 Signal Line

Pin No.	Pin Name	Type	Pin Description
42/60 55/47	CTS0/CTS1 CTS2/CTS3	Input	MODEM signal, clear to transmit, active low, built-in pull-up resistor
41/59 54/46	DSR0/DSR1 DSR2/DSR3	Input	MODEM signal, data device ready, active low, built-in pull-up resistor
40/58 53/45	RI0/RI1 RI2/RI3	Input	MODEM signal, ringing indication, active low, built-in pull-up resistor
39/57 52/44	DCD0/DCD1 DCD2/DCD3	Input	MODEM signal, carrier detection, active low, built-in pull-up resistor
38/56 51/43	RXD0/RXD1 RXD2/RXD3	Input	Asynchronous serial data input, built-in pull-up resistor
80/83 88/91	DTR0/DTR1 DTR2/DTR3	Output	MODEM signal, data terminal ready, active low
79/82 85/90	RTS0/RTS1 RTS2/RTS3	Output	MODEM signal, request to transmit, active low
78/81 84/89	TXD0/TXD1 TXD2/TXD3	Output	Asynchronous serial data output
76/75	OUT0/OUT1	Output	MODEM control output signal (OUT1 of MCR register), active low
74/73	TNOW0/TNOW1	Output	The serial port is transmitting status output (half-duplex transceiver switching), active high

4.4 Print Port Signal Line

Pin No.	Pin Name	Type	Pin Description
62-69	D7～D0	3-state bidirectional	8-bit parallel data output and input, built-in pull-up, connected to DATA7~DATA0
92	STB	Output	Data strobe output, active low, connected to STROBE
93	AFD	Output	Automatic line wrap output, active low, connected to AUTO-FEED
95	INIT	Output	Initialize the printer, active low, connected to INIT
94	SIN	Output	Select the printer, active low, connected to SELECT-IN
34	ERR	Input	Printer error, active low, built-in pull-up, connected to ERROR or FAULT
36	SELT	Input	Printer online, active high, built-in pull-up, connected to SELECT or SELT
35	PE	Input	The printer is out of paper, active high, built-in pull-up, connected to PEMPTY or PERROR
32	ACK	Input	Printer data reception response, active rising edge, built-in pull-up, connected to ACK
33	BUSY	Input	The printer is busy, active high, built-in pull-up, connected to BUSY

4.5 Auxiliary Signal Line

Pin No.	Pin Name	Type	Pin Description
16	RREF	Input	System reference current input, requires an external 12KΩ resistor to GND
25	XI	Input	Optional, crystal oscillation input terminal, external crystal and oscillation capacitor
24	XO	Input and output	Optional, inverting output terminal of crystal oscillation, external crystal and oscillation capacitor
28	SCL	Output	General-purpose output, clock output of external configuration chip, can be externally connected to the SCL pin of the serial EEPROM configuration chip 24CXX
29	SDA	Open-drain output and input	General-purpose output and input, built-in pull-up resistor, can be connected to the SDA pin of the serial EEPROM configuration chip 24CXX
30	SDX	3-state bidirectional	General-purpose output and input, built-in pull-up resistor
31	SCS	Output	General-purpose output
100	CKSEL	Input	Serial port clock frequency selection input, built-in pull-up resistor
98	4S1P#	Input	Software recognition mode selection input, built-in pull-up resistor
1	GPO	Output	General-purpose output
4	RSVD	Reserved	Pins are reserved and connections are prohibited

5. Configuration

5.1 Global Function Configuration

The CH384 chip has two main hardware function modes: 4 serial ports + parallel port function mode, and 4 serial ports + extended multi-serial port function mode. The pin definitions in the two functional modes are different. This manual only covers the former. For the latter, please refer to Datasheet (2) CH384DS2.PDF.

The 4S1P# pin of the CH384 chip is used to select the software recognition mode:

4S1P# connected to VCC33 or suspended, i.e. 4S1P#=1, then it is 4-serial port mode (parallel/print port is not used);

4S1P# connected to GND, i.e. 4S1P#=0, then it is 4-serial port + print port mode.

The CKSEL pin of the CH384 chip is used to select the clock frequency of the internal 4 serial ports:

CKSEL connected to VCC33 or suspended, i.e. CKSEL=1, the clock is input from the XO pin, the frequency is determined by the external crystal, and the internal frequency coefficient defaults to 1/12 divider, which supports the selection of the 2x frequency again by CK2X or CKnS;

CKSEL connected to GND, i.e. CKSEL=0, then the clock is input from XO pin, the frequency is determined by the external crystal, and the internal frequency coefficient is always forced to 2x frequency;

CKSEL connected to PERST# pin, i.e., CKSEL=R, then the internal crystal oscillator is disabled, and the clock is provided by the internal PLL with a frequency of 125MHz, and the internal frequency coefficient is defaulted to 1/68 divider, which supports to select no divider again by CK2X or CKnS.

5.2 External Configuration Chip

The CH384 chip will check the data in the external 24CXX configuration chip every time it is powered on or the PCIE bus is reset. If the configuration chip is connected and the data is valid, it will automatically be loaded into the CH384 chip to replace the default PCIE identification information.

The configuration chip 24CXX is a 4-pin or 8-pin packaged non-volatile serial EEPROM memory. In addition to providing configuration information to CH384, it can also save some other parameters for the application program. CH384 supports the following models of 24CXX chips: 24C01 (A), 24C02, 24C04, 24C08, 24C16, etc.

The following table is the data definition in the configuration chip 24CXX.

Byte address	Abbreviation	Data usage description	Default value
00H	CFG	External configuration chip valid flag, must be 54H	54H
01H	FREQ	Bits 3 to 0 are used to select the internal frequency coefficients of serial port 3 to serial port 0 respectively.	0FFH
03H-02H	RSVD	(Reserved)	0000H
05H-04H	VID	Vendor ID	Custom
07H-06H	DID	Device ID	Custom
08H	RID	Revision ID	Custom
0BH-09H	CLS	Class Code	070005H
0DH-0CH	SVID	Subsystem Vendor ID	Custom
0FH-0EH	SID	Subsystem ID	Custom
1FH-10H	RSVD	(Reserved)	00H or FFH
Other addresses	APP	User or application custom unit	

5.3 Serial Internal Clock

The CH384 chip has an internal clock oscillator, which can generate the external clock signal required by the serial port through an external crystal and capacitor. If the crystal and capacitor are not connected, then connecting the

CKSEL pin to the PERST# pin can generate the clock required for the serial port through the internal PLL.
CH384 internally divides or multiplies the external clock signal of the XO pin to generate the internal reference clock of each serial port. In order to be compatible with the 16C550 chip of the existing computer serial port, the default internal clock frequency is 1.8432MHz, and the corresponding maximum serial port baud rate is 115200bps. The CH384 chip supports multiple internal clock frequencies. When the internal clock frequency doubles, if the application software remains unchanged, the actual communication baud rate also doubles, that is, the serial port set to 115200bps by the application software is actually 230400bps.
The serial port of CH384 can select the frequency division or frequency multiplication coefficient through the CKSEL pin or the CFG/FREQ flag bit in the external configuration chip, converting the frequency of the external clock into two internal clock frequencies, thereby supporting more and larger serial port bauds Rate. The following table shows the internal clock frequency and maximum serial port baud rate of the serial port based on the CKSEL pin, CFG/FREQ flag and external crystal frequency. CK2X in the table is bit 5 of the IER register of each serial port; CFG in the table refers to the valid flag of the external configuration chip, and CKnS (that is, CK0S ~ CK3S) are bits 0 to 3 of FREQ respectively.

Prerequisites	CKSEL=1	CKSEL=1	CKSEL=R	CKSEL=R
Combination selection	CK2X=0 and CFG valid or CKnS=1	CK2X=1 or CKSEL=0 or CFG valid and CKnS=0	CK2X=0 and CFG invalid or CKnS=1	CK2X=1 or CFG valid and CKnS=0
Internal frequency coefficient	1/12 Frequency division	2 Frequency multiplier	1/68 Frequency division	No frequency division
External crystal frequency 22.1184MHz	1.8432MHz 115.2Kbps	44.2368MHz 2.7648Mbps		
External crystal frequency 0.9216MHz		1.8432MHz 115.2Kbps		
External crystal frequency 11.0592MHz	0.9216MHz 57.6Kbps	22.1184MHz 1.3824Mbps		
External crystal frequency 18.432MHz		36.864MHz 2.304Mbps		
Internal PLL frequency 125MHz			1.8382MHz 114.9Kbps	125MHz 7.8125Mbps

The 114.9Kbps obtained with the internal PLL method of 1/68 division is only 0.27% different from the standard 115.2Kbps, which is acceptable.

6. Register

6.1 Basic Agreement

6.1.1. Attribute abbreviation: R=completely read-only, W=readable and writable, S=read-only but can be set in advance, …=ellipsis.

6.1.2. Number system of data: If it ends with H, it is a hexadecimal number, otherwise it is a binary number.

6.1.3. Numerical wildcards and attributes: r=reserved (forbidden to use), x=any value, …=ellipsis.

6.2 PCIE Configuration Space

Address	Register Name	Register Properties	Default value after system reset
01H-00H	Vendor ID	SSSS	1C00H
03H-02H	Device ID	SSSS	4 serial ports: 3470H 4 serial ports + parallel port: 3450H 4 serial ports expanded 8 strings: 3853H 4 serial ports expanded 28 strings: 4353H
05H-04H	Command	RRRRRWRRRRRRRWWW	0000000000000000
07H-06H	Status	RRRRRRRRRRRRRRRR	000000000001x000
08H	Revision ID	SS	10H
0BH-09H	Class Code	SSSSSS	070005H
0FH-0CH		RRRRRRRR	00000000H
13H-10H	I/O Base Address 0	WWWWWWWWWWWWWWWW WWWWWWWWRRRRRRRR	0000000000000000 0000000000000001
17H-14H		RRRRRRRR	00000008H
1BH-18H	I/O Base Address 2	WWWWWWWWWWWWWWWW WWWWWWWWWWWWWWRR	0000000000000000 0000000000000001
2BH-1CH		RRRR….RRRR	0000….0000H
2DH-2CH	Subsystem Vendor ID	SSSS	Same as VID
2FH-2EH	Subsystem ID	SSSS	Same as DID
33H-30H		RRRRRRRR	00000001H
34H		RR	60H
3BH-35H		RRRR….RRRR	0000….0000H
3FH-3CH	Interrupt Line & Pin	RRRRRRRRRRRRRRRR RRRRRRRRWWWWWWWW	0000000000000000 0000000100000000
FFFH-40H	Reserved	(Disabled)	(Disabled)

6.3 I/O Base Address Register

Offset address	Register Name	Register Properties	Default value after system reset
3FH-00H	Map to 8 serial port registers (8*8 bytes) of the external expansion 0#CH438 chip	WW	0FFH
7FH-40H	Map to 8 serial port registers (8*8 bytes) of the external expansion 1#CH438 chip	WW	0FFH
BFH-80H	Map to 8 serial port registers (8*8 bytes) of the external expansion 2#CH438 chip	WW	0FFH
C7H-C0H	8 serial port registers of internal serial port 0	WW	XXH
CFH-C8H	8 serial port registers of internal serial port 1	WW	XXH
D7H-D0H	8 serial port registers of internal serial port 2	WW	XXH
DFH-D8H	8 serial port registers of internal serial port 3	WW	XXH
E0H	Map to the interrupt special status register of the external expansion 0#CH438 chip	RR	00H
E3H-E1H	Reserved	(Disabled)	0FFH
E4H	Map to the interrupt special status register of the external expansion 1#CH438 chip	RR	00H
E5H	Reserved	(Disabled)	0FFH
E6H	Map to the interrupt special status register of the external expansion 2#CH438 chip	RR	00H
E7H	Reserved	(Disabled)	0FFH
E8H	General-purpose output register GPOR	WWRRRWWW	00rrr111
E9H	Internal interrupt status register IINT	RRRRRRRR	0rrr0000
EAH	General-purpose input register GPIR	RRRRRRRR	1xxr1rr1
EBH	External interrupt status register XIN	RRRRRRWR	111rrr0r
F7H-ECH	Reserved	(Disabled)	xxH
F8H	Control and status register CTRL	WRRRRRRR	1rrxrrrr
FFH-F9H	Reserved	(Disabled)	xxH

6.4 Bit of Register

Register Name	Bit Address	Attributes	Bit usage instructions (Default value)	Bit value=0	Bit value =1
General-purpose output register GPOR (I/O base address 0+0E8H address)	Bit 0	W	Set output value of SDA pin (1)	Low	High
	Bit 1	W	Set output value of SCL pin (1)	Low	High
	Bit 2	W	Set output value of SCS pin (1)	Low	High
	Bit 6	W	Set the data direction of SDX pin (0)	Input	Output
	Bit 7	W	Set output value of SDX (0)	Low	High
Internal interrupt status register IINT (I/O base address 0+0E9H address)	Bit 0	R	Interrupt status of internal serial port 0 (0)	No interrupt	Interrupting
	Bit 1	R	Interrupt status of internal serial port 1 (0)	No interrupt	Interrupting
	Bit 2	R	Interrupt status of internal serial port 2 (0)	No interrupt	Interrupting
	Bit 3	R	Interrupt status of internal serial port 3 (0)	No interrupt	Interrupting
	Bit 7	R	Interrupt status of internal print port (0)	No interrupt	Interrupting
General-purpose input register GPIR (I/O base address 0+0EAH address)	Bit 0	R	Input status of SDA pin (1)	Low	High
	Bit 3	R	Input status of INT# pin (1)	Low	High
	Bit 5	R	Input status of CKSEL (X)	Low	High
	Bit 6	R	Input status of MDSEL (X)	Low	High
	Bit 7	R	Input status of SDX (1)	Low	High
External interrupt status register XINT (I/O base address 0+0EBH address)	Bit 1	W	Set global interrupt enable (0)	Disable interrupt	Enable interrupt
	Bit 5	R	Input status of INT0# pin (1)	Low	High
	Bit 6	R	Input status of INT1# pin (1)	Low	High
	Bit 7	R	Input status of INT2# pin (1)	Low	High
Control and status register CTRL (I/O base address 0+0F8H address)	Bit 4	R	Input XO pin status (X)	Low	High
	Bit 7	W	Set output value of GPO pin (1)	Low	High

6.5 Serial Port Register

The serial port of CH384 is compatible with the industrial standard 16550 or 16C750 and has been enhanced. The register bits marked in gray in the table are enhanced functions, and the FIFO buffer length has been extended to 256 bytes. For other registers, please refer to the single serial port chip 16C550 or dual serial port chip. Description of serial port chip CH432 or eight serial port chip CH438. The actual address of the serial port 0 register is I/O base address 0, add 0C0H first, and then add the offset address in the table. The actual address of the serial port 1 register is I/O base address 0, add 0C8H first, and then add the offset address in the table. The actual address of the serial port 2 register is I/O base address 0 first plus 0D0H and then the offset address in the table. The actual address of the serial port 3 register is I/O base address 0 plus 0D8H plus the offset address in the table. The registers of each serial port are the same. DLAB in the table is bit 7 of the register LCR. X indicates that the DLAB value is not cared for, RO indicates that the register is read-only, WO indicates that the register is write-only, and R/W indicates that

the register is readable and writable.

Address	DLAB	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	RO	RBR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	WO	THR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	R/W	IER	RESET	LOWPOWER	CK2X	0	IEMODEM	IELINES	IETHRE	IERECV
2	X	RO	IIR	FIFOENS	FIFOENS	TRIG16	0	IID3	IID2	IID1	NOINT
2	X	WO	FCR	RECVTG1	RECVTG0	TRIG16	0	0	TFIFORST	RFIFORST	FIFOEN
3	X	R/W	LCR	DLAB	BREAKEN	PARMODE1	PARMODE0	PAREN	STOPBIT	WORDSZ1	WORDSZ0
4	X	R/W	MCR	HALF	0	AFE	LOOP	OUT2	OUT1	RTS	DTR
5	X	RO	LSR	RFIFOERR	TEMT	THRE	BREAKINT	FRAMEERR	PARERR	OVERR	DATARDY
6	X	RO	MSR	DCD	RI	DSR	CTS	△DCD	△RI	△DSR	△CTS
7	X	R/W	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	R/W	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	R/W	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

The following table is the default value of the serial port register after power-on reset or PCIE bus reset or serial port soft reset.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IER	0	0	0	0	0	0	0	0
IIR	0	0	0	0	0	0	0	1
FCR	0	0	0	0	0	0	0	0
LCR	0	0	0	0	0	0	0	0
MCR	0	0	0	0	0	0	0	0
LSR	0	1	1	0	0	0	0	0
MSR	DCD	RI	DSR	CTS	0	0	0	0
SCR	Holding	Holding	Holding	Holding	Holding	Holding	Holding	Holding
FIFO	Reset, including transmit FIFOs and receive FIFOs							
TSR	Reset, TSR is the serial port transmit shift register							
RSR	Reset, RSR is the serial port receive shift register							
Others	Undefined							

RBR: Receive buffer register. If the DATARDY bit of LSR is 1, the received data can be read from this register. If FIFOEN is 1, the data received from the serial port shift register RSR is first stored in the receive FIFO and then read out through this register.

THR: Transmit holding register, including transmit FIFO, used to write data to be sent. If FIFOEN is 1, the written data is first stored in the transmit FIFO, and then output one by one through the transmit shift register TSR.

IER: Interrupt enable register, including enhanced function control bits and serial port interrupt enable.

RESET: If this bit is set to 1, the serial port is soft reset. This bit can be cleared to 0 automatically without software clearing it.

LOWPOWER: If this bit is 1, the internal reference clock of the serial port is turned off, thereby putting the serial port into a low power consumption state.

CK2X: If this bit is 1, the external clock signal is forced to be multiplied by 2 and used as the internal reference clock of the serial port, and is not controlled by the FREQ bit CKnS.

IEMODEM: Setting this bit to 1 allows modem input status change interrupts.

IELINES: This bit is 1 to allow receiving line status interrupts.

IETHRE: If this bit is 1, the holding register empty interrupt is allowed to be sent.
IERECV: If this bit is 1, data interrupt is allowed to be received.
IIR: Interrupt identification register, used to analyze interrupt sources and handle them.
FIFOENS: This bit is the FIFO enable status. If it is 1, it means that the FIFO has been enabled.

IIR register bit				Priority	Interrupt type	Interrupt source	Clear interrupt method
IID3	IID2	IID1	NOINT				
0	0	0	1	None	No interrupt	No interrupt	
0	1	1	0	1	Receive line status	OVERR, PARERR, FRAMEERR, BREAKINT	Read LSR
0	1	0	0	2	Receive data is available	The number of bytes received reaches the FIFO trigger point	Read RBR
1	1	0	0	2	Receive data timeout	The next data has not been received for more than 4 data times.	Read RBR
0	0	1	0	3	THR register empty	The transmit holding register is empty and IETHRE changes from 0 to 1 to re-enable the interrupt.	Read IIR or write THR
0	0	0	0	4	MODEM input change	△CTS, △DSR, △RI, △DCD	Read MSR

FCR: First-in first-out buffer FIFO control register, used to enable and reset the FIFO.
TRIG16: If this bit is 1, the trigger point of the receive FIFO interrupt and hardware flow control is equal to the trigger point of the 16-byte FIFO. This bit is only allowed to be modified when DLAB is 1.
RECVTG1 and RECVTG0: Set the trigger point for interrupt and hardware flow control of the receive FIFO, 00 corresponds to 1 byte, i.e., receiving 1 byte full generates an interrupt for receiving data available and automatically invalidates the RTS pin when enabling hardware flow control.

TRIG16	RECVTG1	RECVTG0	Trigger point
0	0	0	1 byte
0	0	1	32 bytes
0	1	0	128 bytes
0	1	1	224 bytes
1	0	0	1 byte
1	0	1	4 bytes
1	1	0	8 bytes
1	1	1	14 bytes

TFIFORST: If the position 1 is cleared, the data in the transmit FIFO (without TSR) will be cleared, and the bit can be cleared automatically without software clearing.
RFIFORST: A 1 in this position clears the data in the receive FIFO (without RSR), and this bit can clear 0 automatically without software clearing.
FIFOEN: This bit is 1 to enable FIFO, this bit clear 0 to disable FIFO, disable FIFO for 16C450 compatibility mode, equivalent to the FIFO is only one byte (RECVTG1=0, RECVTG0=0, FIFOEN=1), it is recommended to enable FIFO.
LCR: Line Control Register, used to control the format of serial communication.
DLAB: This bit is the divisor latch access enable, a 1 enables access to DLL and DLM, a 0 enables access to RBR/THR/IER.
BREAKEN: A one in this bit forces the generation of a BREAK line interval.

PARMODE1 and PARMODE0: When PAREN is 1 it sets the format of the parity bit: 00 for odd parity, 01 for even parity, 10 for the flag bit (MARK, set to 1), and 11 for the blank bit (SPACE, clear to 0).
PAREN: a 1 for this bit allows parity bits to be generated on transmit and checked on receive, a 0 for no parity bits.
STOPBIT: a 1 for this bit allows two stop bits, a 0 for one stop bit.
WORDSZ1 and WORDSZ0: Set the word length, 00 is 5 data bits, 01 is 6 data bits, 10 is 7 data bits, 11 is 8 data bits.
MCR: MODEM control register, used to control MODEM output.
HALF: If this bit is 1, it enters half-duplex transceiver mode, with priority for transmitting, and reception when not transmitting. In half-duplex mode, the DTR pin always outputs the transmitting status TNOW, which can be used to control RS485 transceiver switching. This bit is only allowed to be modified when DLAB is 1.
AFE: Setting this bit to 1 allows CTS and RTS hardware automatic flow control. If AFE is 1, then the serial port will continue to transmit the next data only when it detects that the CTS pin input is valid (low level is active), otherwise the serial port transmission will be suspended. When AFE is 1, the CTS input state change will not generate a MODEM state. Interrupt. If AFE is 1 and RTS is 1, then when the receiving FIFO is empty, the serial port will automatically invalidate the RTS pin (active low level). The serial port will automatically invalidate the RTS pin until the number of bytes received reaches the trigger point of the FIFO, and is able to assert the RTS pin again when the receive FIFO is empty. Using hardware automatic rate control, you can connect your own CTS pin to the other party's RTS pin, and transmit your own RTS pin to the other party's CTS pin.
LOOP: If this bit is 1, the test mode of the internal loop is enabled. In the test mode of the internal loop, all external output pins of the serial port are in an invalid state, TXD returns to RXD internally (that is, the output of TSR returns to the input of RSR internally), RTS returns to CTS internally, and DTR returns to DSR and OUT1 internally. Internally returns to RI, OUT2 internally returns to DCD.
OUT2: If this bit is 1, the interrupt request output of the serial port is allowed, otherwise the serial port does not generate an actual interrupt request.
OUT1: This bit is a user-definable MODEM control bit. In the 4 serial ports + extended serial port mode, the actual output pin is not connected. In the 4 serial ports + parallel port mode, the corresponding output pins of serial port 0 and serial port 1 are OUT0 and OUT1 pins.
RTS: A 1 in this bit makes the RTS pin output valid (active low), otherwise the RTS pin output is invalid.
DTR: If this bit is 1, the output of DTR pin is valid (active low), otherwise the output of DTR pin is invalid.
LSR: Line Status Register, used to analyze the serial port status in query mode.
RFIFOERR: A one in this bit indicates that there is at least one PARERR, FRAMEERR, or BREAKINT error in the receive FIFO.
TEMT: A one in this bit indicates that the Transmit Holding Register THR and Transmit Shift Register TSR are all empty.
THRE: A one in this bit indicates that the transmit hold register THR is empty.
BREAKINT: A one in this bit indicates that a BREAK line interval was detected.
FRAMEERR: A one in this bit indicates a framing error for the data being read from the receive FIFO, missing a valid stop bit.
PARERR: A one in this bit indicates a parity error for the data being read from the receive FIFO.
OVERR: A one in this bit indicates a receive FIFO buffer overflow.
DATARDY: A 1 in this bit indicates that there is received data in the receive FIFO, and this bit is automatically cleared to 0 after all data in the FIFO is read.
MSR: MODEM Status Register, used to query the MODEM status.
DCD: This bit is the bit inverse of the DCD pin, a 1 indicates that the DCD pin is valid (active low).
RI: This bit is the bit inverse of the RI pin, a value of 1 indicates that the RI pin is valid (active low).

DSR: This bit is the bit inverse of the DSR pin, a one indicates that the DSR pin is valid (active low).
CTS: This bit is the bit inverse of the CTS pin, a 1 indicates that the CTS pin is valid (active low).
△DCD: A one in this bit indicates that the input state of the DCD pin has changed.
△RI: A one indicates that the input status of the RI pin has changed.
△DSR: A one indicates that the input state of the DSR pin has changed.
△CTS: A one indicates that the input state of the CTS pin has changed.
SCR: User definable register.
DLL and DLM: Baud rate divisor latches, DLL is the low byte and DLM is the high byte, both of which form a 16-bit divisor used in a serial port baud rate generator consisting of a 16-bit counter. This divisor = serial port internal reference clock / 16 / desired communication baud rate. If the serial port internal reference clock is 1.8432MHz and the required baud rate is 9600bps, the divisor = 1843200/16/9600 = 12.

6.6 Parallel Port Register

The parallel port of CH384 is compatible with the SPP standard print port and has been enhanced. The register bits marked in gray in the table are enhanced functions. The actual address of the parallel port register is the I/O base address 2 plus the offset address in the table. The parallel port of CH384 mainly has four working modes: SPP (including Nibble, Byte and PS/2), EPP and ECP. The mode ALL in the table refers to all modes, ADV refers to EPP and ECP, RO means register read-only, and WO means the register is write-only, R/W means the register is readable and writable.

Address	Method	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	SPP	RO	PIR	D7IN	D6IN	D5IN	D4IN	D3IN	D2IN	D1IN	D0IN
0	ADV	RO	PIR	IBD7	IBD6	IBD5	IBD4	IBD3	IBD2	IBD1	IBD0
0	ALL	WO	PDR	D7OUT	D6OUT	D5OUT	D4OUT	D3OUT	D2OUT	D1OUT	D0OUT
1	SPP	RO	PSR	!BUSY	ACK	PE	SELT	ERR	!INTFLAG	1	1
1	EPP	RO	PSR						1	1	!EPPREQ
1	ECP	RO	PSR						!ECPICMD	!ECPIBF	!ECPOUT
2	ALL	R/W	PCR	1	1	DIRIN	INTEN	!SIN	INIT	!AFD	!STB
3	SPP	R/W	PXR	0	0	0	0	0	0	0	0
3	EPP	R/W	PXR	0	0	0	0	EPPADDR	MODEEPP	0	0
3	ECP	R/W	PXR	0	0	0	ECPINTF	0	0	ECPDIRIN	MODEECP

The following table is the default value of the parallel port register after power-on reset or PCIE bus reset.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PIR	1	1	1	1	1	1	1	1
PDR	0	0	0	0	0	0	0	0
PSR	!BUSY	ACK	PE	SELT	ERR	1	1	1
PCR	1	1	0	0	0	0	0	0
PXR	0	0	0	0	0	0	0	0
Others	Undefined							

PIR: Data Input Register, used to input real-time data from pins D7-D0 in SPP mode, and data in the input/upload buffer that has been latched in EPP or ECP mode. In EPP mode, this data is latched when the AFD pin or the SIN pin outputs a low level, and in ECP mode, this data is latched when the ACK pin goes low, and also latches !ECPICMD.
PDR: Data output register, used to write data to be output/downloaded. Writing to this register in SPP mode will directly output to the D7-D0 pin; writing to this register in EPP or ECP mode will automatically execute the

handshake protocol of data output or data input.

PSR: Status register, used to query input pins and operation execution status.

!BUSY: This bit is the inverse value of the state of the input pin BUSY in SPP, EPP and ECP modes. When the BUSY pin inputs a high level, this bit is 0.

ACK: This bit is the status of input pin ACK in SPP, EPP and ECP mode.

PE: This bit is the status of input pin PE in SPP, EPP and ECP mode.

SELT: This bit is the status of input pin SELT in SPP, EPP and ECP mode.

ERR: This bit is the state of input pin ERR in SPP, EPP and ECP mode.

!INTFLAG: This bit is the inverse value of the interrupt flag in SPP mode. When the rising edge of the ACK pin generates the interrupt flag, this bit is automatically cleared to 0. After reading the PSR register, this bit is automatically set to 1.

!EPPREQ: This bit is the inverse value of the access operation progress flag in EPP mode. When writing to the PDR register, this bit is automatically cleared to 0, and an EPP access operation is started. This bit is not automatically set to 1 until the operation is completed.

!ECPICMD: This bit is the inverse value of the command flag during reverse transmission in ECP mode. When the reverse transmission is a command, this bit is 0.

!ECPIBF: This bit is the inverse value of the upload buffer full flag for reverse transmission in ECP mode. When the upload buffer is full, this bit is automatically cleared to 0. This bit is automatically set to 1 after reading the PIR register.

!ECPOUT: This bit is the inverse of the flag for forward transfer operation proceeding in ECP mode. When writing to the PDR register, this bit is automatically cleared to 0 and the ECP forward output operation is started to be attempted until the operation is completed, and then this bit is automatically set to 1.

PCR: Control register used to control the output pins and transfer direction as well as interrupt enable.

DIRIN: This bit is the tri-state output control for bi-directional data lines D7-D0 in SPP, EPP and ECP modes, clearing 0 allows tri-state output on pins D7-D0, and setting 1 disables tri-state output on pins D7-D0.

INTEN: This bit is the PCIE interrupt output enable, set to 1 to allow output interrupt request, clear to 0 to disable output interrupt request.

!SIN: A 1 in this bit enables the output of SIN pin (active low), otherwise the output of SIN pin is invalid.

INIT: A 1 in this bit invalidates the INIT pin output, otherwise the INIT pin output is valid (active low).

!AFD: A 1 in this bit will make the output of AFD pin valid (active low), otherwise the output of AFD pin is invalid.

!STB: A 1 in this bit makes the STB pin output valid (active low), otherwise the STB pin output is invalid.

PXR: Setting register, used to set the parallel port working mode.

EPPADDR: This bit is the target space selection in EPP mode. If it is 1, it corresponds to the address access operation of EPP, and if it is 0, it corresponds to the data access operation of EPP.

MODEEPP: If this bit is 1, the EPP mode is enabled.

ECPINTF: This bit is the interrupt flag in ECP mode. When the falling edge of the ERR pin generates the interrupt flag, this bit is automatically set to 1. After reading the PXR register, this bit is automatically cleared to 0.

ECPDIRIN: This bit is the transmission direction control in ECP mode. If it is 0, it corresponds to ECP forward transmission/output, and if it is 1, it corresponds to ECP reverse transmission/input.

MODEECP: If this bit is 1, the ECP mode is enabled.

7. Function Description

7.1 Query and Interrupt

The four serial ports and parallel ports of the CH384 chip share a PCIE interrupt request pin, so after entering the PCIE interrupt service routine, you should first analyze whether the interrupt is requested for CH384 and which serial port or parallel port the interrupt request is. After entering the interrupt service routine, there are two methods: dedicated status analysis and sequential query:

Dedicated status analysis refers to first reading the IINT internal interrupt status register. A valid IINT bit 0 mark indicates a serial port 0 interrupt. A valid IINT bit 1 mark indicates a serial port 1 interrupt. A valid IINT bit 2 mark indicates a serial port 2 interrupt. IINT bit 3 indicates a serial port 2 interrupt. If the flag is valid, it indicates serial port 3 interrupt. If the IINT bit 7 flag is valid, it indicates parallel port interrupt. It will be processed directly and exit based on the analysis results. If there is no interruption, it will exit directly.

Sequential query means first read the PSR or PXR register of parallel port, if it is ECP mode then check the ECPINTF flag of PXR register, otherwise check the !INTFLAG flag of PSR register, if it is valid then it means there is an interrupt, process it and exit, if there is no interrupt, then read IIR register of serial port 0, if there is an interrupt then process it and exit, if there is no interrupt then read IIR register of serial port 1, if there is no interrupt then process it and exit, if there is no interrupt then read IIR register of serial port 3, if there is no interrupt then process it and exit. IIR register of serial port 1, if there is an interrupt then process and exit, without interrupt then read IIR register of serial port 2, if there is an interrupt then process and exit, without interrupt then read IIR register of serial port 3, if there is an interrupt then process and exit, without interrupt then exit directly.

After confirming that it is an interrupt of a certain serial port, if necessary, you can further analyze the LSR register to analyze the cause of the interrupt and handle it.

If the serial port works in interrupt mode, you need to set the IER register to allow the corresponding interrupt request, and set OUT2 in the MCR register to allow interrupt output.

If the parallel port works in interrupt mode, INTEN of the PCR register needs to be set to allow interrupt output. Among them, the SPP or EPP mode starts the interrupt request with the rising edge of the ACK pin, and the ECP mode starts the interrupt request with the falling edge of the ERR pin.

If the serial port works in query mode, there is no need to set OUT2 of IER and MCR. You only need to query the LSR register and analyze and process it.

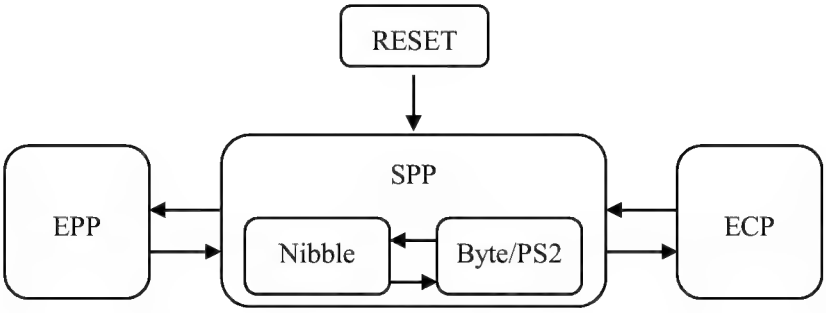
If the parallel port works in query mode, there is no need to set INTEN of PCR, only the PSR and PXR registers need to be queried and analyzed.

7.2 Serial Port Operation

For specific operations, please refer to the instructions for the single serial port chip 16C550, the dual serial port chip CH432, or the eight serial ports chip CH438.

7.3 Parallel Port Operation

The three working modes of CH384 parallel port are mutually exclusive, and the default is SPP mode. In SPP mode, additional modes such as Nibble, Byte and PS/2 can be implemented. You can also switch back and forth between SPP, EPP or ECP modes by setting the PXR register. The following is a diagram of parallel port working mode switching.



In SPP mode, software can be used to control PCR and query PSR to realize transmission of Nibble, Byte and PS/2. For specific operation steps, please refer to the IEEE1284 specification.

In EPP mode, you should select the target space through EPPADDR of PXR, set the transmission direction through DIRIN of PCR, and then write data to PDR (for reverse transmission, you can write any data) start EPP transmission, and query PSR until !EPPREQ is 1; if it is reverse transmission, the data needs to be read from the PIR (it is recommended to read together with the PSR to improve efficiency).

In ECP mode, the transmission direction should be set through DIRIN of PCR and ECPDIRIN of PXR. For forward transmission, you can write data to PDR to start ECP forward transmission, and query PSR until !ECPOUT is 1; for reverse transmission, you can Directly query PSR until !ECPIBF is 0, and then read data from PIR (it is recommended to read together with PSR to improve efficiency, and obtain !ECPICMD from PSR).

7.4 Application Description

The CH384 chip's serial output pins are all 3.3V LVCMOS levels, compatible with 5V TTL levels, and the input pins are able to tolerant 5V voltage, compatible with 5V CMOS levels, 3.3V LVCMOS and 5V TTL and LVTTL levels, and can be further converted to RS232 serial ports with the addition of an RS232 level converter.

The pins of the CH384 chip in UART mode include: data transmission pins and MODEM contact signal pins. Data transmission pins include: TXD pin and RXD pin, both of which are high level by default. MODEM contact signal pins include: CTS pin, DSR pin, RI pin, DCD pin, DTR pin, RTS pin and OUT pin of some serial ports in 4 serial ports + parallel port mode. The default is high level. All these MODEM contact signals can be used as general IO pins, controlled and defined by computer applications.

The CH384 has built-in independent transceiver buffers and FIFOs to support simplex, half-duplex or full-duplex asynchronous serial communication. The serial data includes 1 low level start bit, 5, 6, 7 or 8 data bits, 0 or 1 additional parity or flag bit, 1 or 2 high level stop bits, and supports odd/even/flag/blank parity.CH384 supports the commonly used baud rates of 1200, 2400, 4800, 9600, 19.2K, 38.4K, 57.6K, 115.2K, 230.4K, 460.8K, 115.2K, 230.4K, 460.8K, 115.2K, 230.4K, 460.8K, 115.2K, 460.4K, 460.4K, 460.4K, 460.8K, 115.2K, 230.4K, 460.8K, 921.6K, 1.8432M, 2.7648M, 7.8125M and so on. The baud rate error of the serial port transmitting signal is less than 0.2%, and the allowable baud rate error of the serial port receiving signal is not less than 2%.

Under the Windows and Linux operating systems on the computer side, the CH384 driver is compatible with standard serial ports, so most of the original serial port applications are fully compatible and usually do not require any modification.

The parallel port output pins of the CH384 chip are all 3.3VLVCMOS levels, compatible with 5VTTL levels, and the input pins can tolerant 5V voltage, and are compatible with 5VCMOS levels, 3.3VLVCMOS, 5VTTL and LVTTL levels. The pins of the CH384 chip in parallel port mode include: bidirectional data pins, control output pins and status input pins. Bidirectional data pins and control output pins, except the INIT pin, are all high by default. In SPP mode, all these signals can be used as general IO pins, controlled and defined by the computer application.

Under Windows and Linux operating systems on the computer side, the CH384 driver is compatible with standard serial ports and standard print ports, so most of the original serial port applications and parallel port applications are

fully compatible and usually do not require any modification. CH384 can be used to expand additional high-speed RS232 serial ports and parallel ports/print ports for computers through the PCIE bus, high-baud rate serial ports that support automatic hardware rate control, RS422 or RS485 communication interfaces, SIR infrared communication interfaces, etc.

8. Parameters

8.1 Absolute Maximum Value (Critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

Name	Parameter Description		Min.	Max.	Unit
TA	Ambient temperature during operation	CH384P	-40	85	℃
		CH384L	-40	85	℃
TS	Ambient temperature during storage		-55	125	℃
VCC33	I/O power voltage (VCC33 to power, GND to ground)		-0.4	4.2	V
VCC18 VCC18A	Core power voltage (VCC18 to power, GND to ground) Transmitting power voltage (VCC18A to power, GND to ground)		-0.4	2.3	V
VIO	Voltage on the PCIE signal and each auxiliary signal input or output pin		-0.4	VCC33+0.4	V
VIO5	Voltage on serial and parallel ports and expansion input or output pins		-0.4	5.3V	V

8.2 Electrical Parameters (Test conditions: TA=25℃, VCC33=3.3V, does not include pins to connect to PCIE bus)

Name	Parameter Description	Min.	Typ.	Max.	Unit
VCC33	I/O power voltage	3.0	3.3	3.6	V
VCC18 VCC18A	Core power voltage Transmitting power voltage	1.65	1.8	1.95	V
ICC	Total supply current during operation	2	90	270	mA
VIL	Low level input voltage	-0.4		0.7	V
VIH	High level input voltage	2.0		VCC33+0.4	V
VOL	Low level output voltage (4mA input current)			0.4	V
VOH	High level output voltage (4mA output current)	VCC33-0.4			V
IIN	Input current without pull-up input			10	uA
IUP	Input current with pull-up input	20	40	100	uA

8.3 Timing Parameters (Test conditions: TA=25℃, VCC33=3.3V, refer to figure below)

Name	Parameter Description	Min.	Typ.	Max.	Unit
FCLK	CLK input frequency (Main frequency of PCIE bus)	0	100	105	MHz
FSCL2	SCL output frequency when the 2-wire interface is automatically loaded		244	260	KHz
FSCL3	SCL output frequency when 3-wire interface is automatically loaded		31	35	MHz
FXI	XI input frequency, crystal frequency	0.9216	22.1184	64	MHz

9. Applications

9.1 4 Serial Ports + Parallel Port (Figure Below)

This is the basic circuit of PCIE four serial ports + parallel port/print port based on the CH384 chip. The RS232 level conversion chip is not included in the picture.

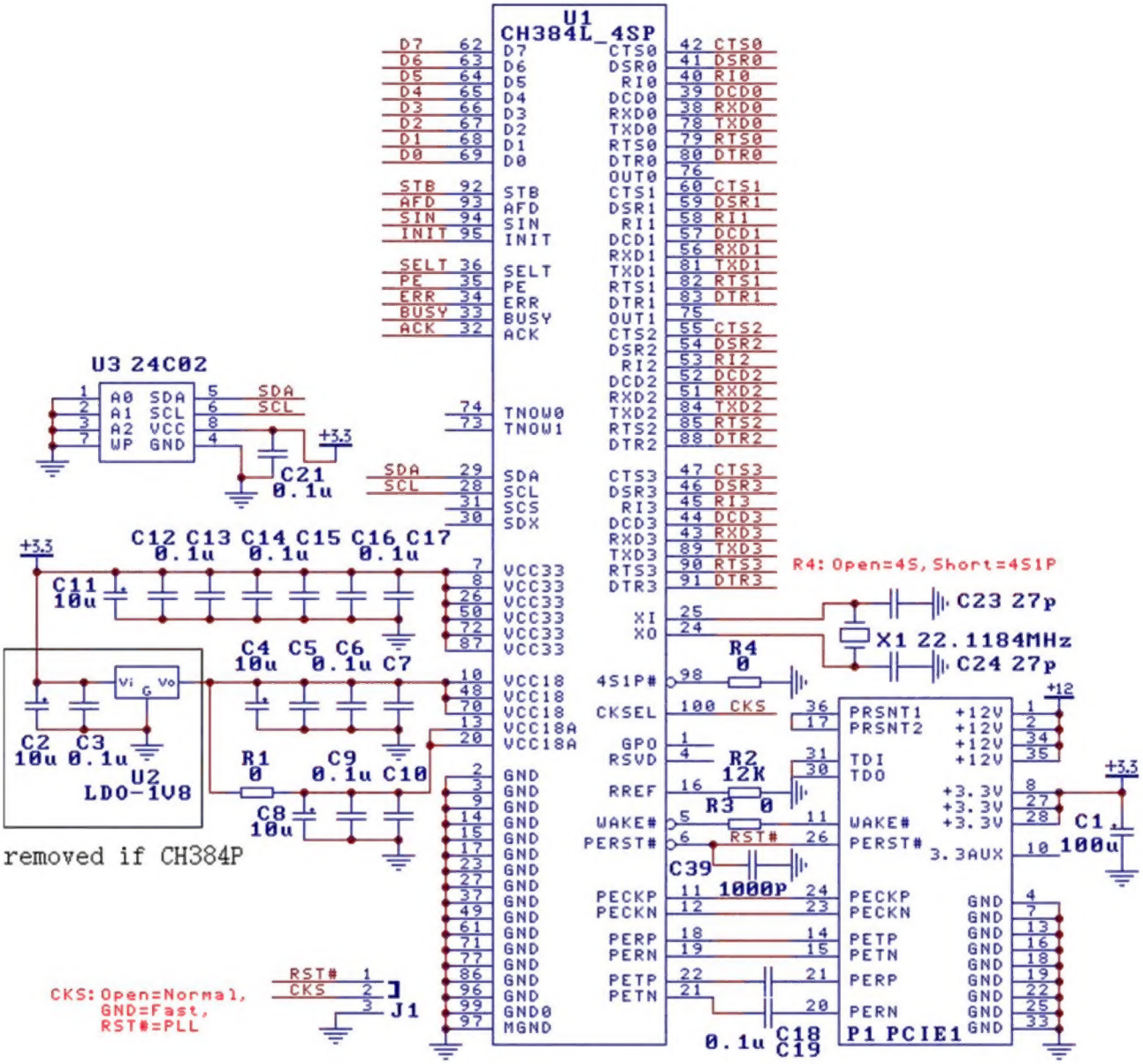
U3 is an optional external configuration chip, and the website provides online configuration tool software under Windows system.

IEEE1284 requires that the print port signal maintains impedance matching. Therefore, the parallel data line of the print port may require a series resistor and a parallel capacitor, which can be omitted when the requirements are not high.

Crystal X1 and capacitors C23 and C24 are used in the clock oscillation circuit. Capacitor C39 is used for power-on reset, and other capacitors are used for power supply decoupling. The 10uF capacitor is an MLCC or tantalum capacitor, and the 0.1uF capacitor is a high-frequency capacitor, which are connected in parallel to the power pin of CH384.

For the CH384P chip, the LDO buck is built-in, so U2, C2 and C3 must be removed.

CH384 is a high-frequency circuit. When designing the PCB board, please refer to the PCIE bus specification or the PCIE_PCB.PDF.


U1
CH384L_4SP
U3 24C02
A0 SDA
A1 SCL
A2 VCC
WP GND
SDA
SCL
+3.3
C21
0.1u
C12 C13 C14 C15 C16 C17
0.1u 0.1u 0.1u
C11
10u
C4 C5 C6
10u 0.1u C7
C2 C3
10u 0.1u
U2
LDO-1V8
R1
0
C9
0.1u C10
C8
10u
removed if CH384P
R4: Open=4S, Short=4S1P
C23 27p
X1 22.1184MHz
C24 27p
R4
0
R2
12K
R3 0
RST#
C39
1000p
PRSNT1
PRSNT2
TDI
TDO
WAKE#
PERST#
3.3AUX
PECKP
PECKN
PETP
PETN
PERP
PERN
P1 PCIE1
C1
100u
CKS: Open=Normal,
GND=Fast,
RST#=PLL
J1
0.1u C18
C19